Characteristics of digital ICs (1)

ICs are usually evaluated by comparing the characteristics of the basic gates in each Ic. The different characteristics are —

i) **Propogation Time delay**

This is the average transition delay time for the signal to propagate from input to output when the signal changes its value. This determines how fast the logic system can operate.

ii) **Fan-in and Fan-out**

The maximum no. of inputs which can be applied to a logic gate is known as Fan-in. On the other hand, Fan-out of a logic gate is the number of gates than can be driven by it.

iii) **Noise margin**

The maximum value of noise signal that a system can reject with performance unaffected is called Noise margin.

iv) **Noise immunity**

The ability of the circuit to tolerate noise signals.

v) **Power dissipation**

It is defined as the power consumed by the gate, which must be available from the power supply. Power dissipation of a gate should be as small as possible.

Digital Logic Families

Integrated circuits or ICs can be used as logic circuits which are classified into 3 main classes -

i) Small Scale Integrated circuits (SSI)

Those ICs which have total number of gates less than 12 on the same chip

ii) Medium scale ICs (MSI)

Those ICs which have total number of gates 12 to 100 on the same chip are called MSI.

iii) Large Scale ICs (LSI)

Those ICs which have total number of gates more than 100 on the same chip are called LSI.

Digital Logic families are divided into 2 types -

i) Bipolar logic families

Bipolar logic families are subdivided into 2 groups -

a) Saturated bipolar logic

Members of this family are -

→ RTL - Resistor - Transistor logic
→ TTL - Transistor - Transistor logic
→ DTL - Diode - Transistor logic

b) Non - saturated bipolar logic

Members of this family are -

→ TTL Schottky
→ ECL - Emitter coupled logic

(iii) Unipolar Logic families

→ COMS - Complementary Metal-oxide semiconductor

→ MOS - Metal-oxide semiconductor

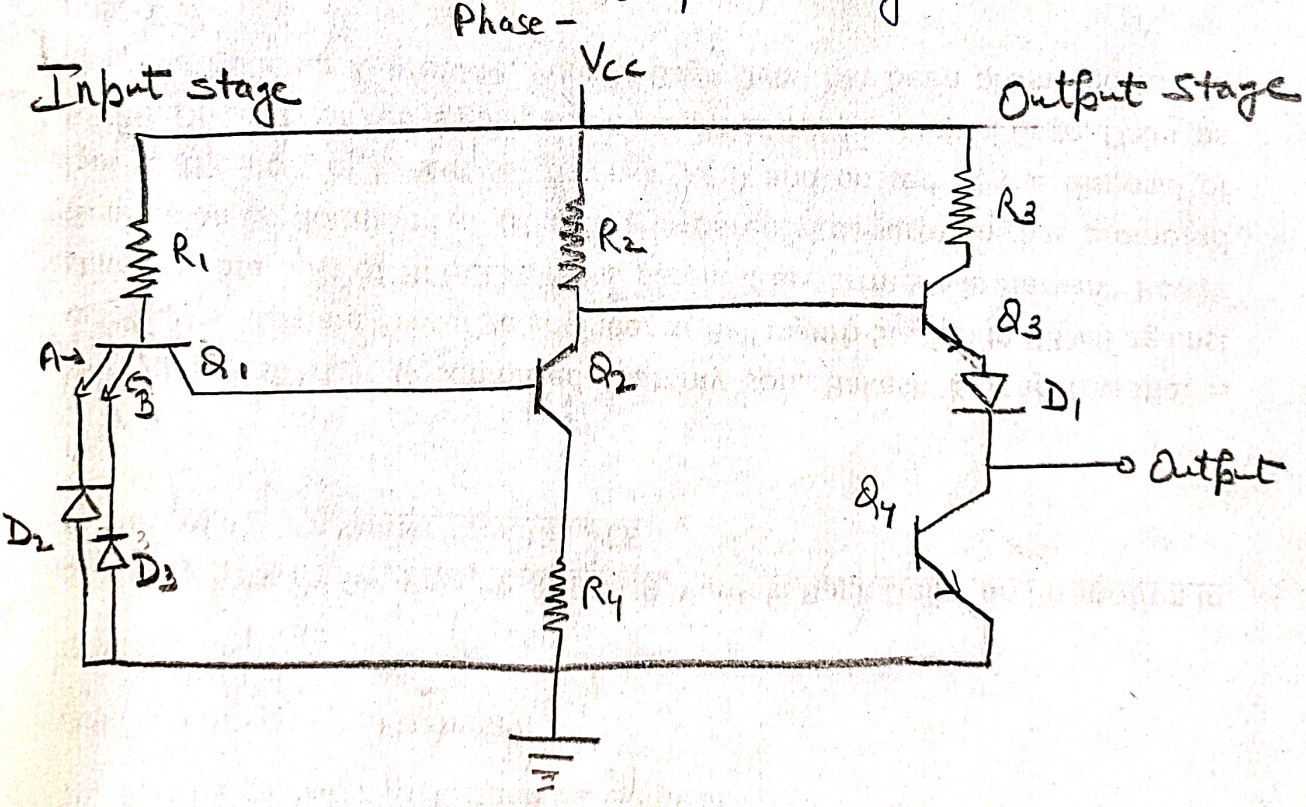
Transistor-Transistor Logic (TTL)

TTL is the most popular & widely used amongst all logic families because of its speed, good fan-in and fan-out.

TTL circuit can be used as a NAND gate.

→ The transistor is basic building block of TTL.

→ It has 3 parts - Input stage, Phase-splitter and Output stage.



In input stage, we have transistor Q_1 which is utilised as a multi-emitter, as there are two inputs connected (A & B) at the emitter of transistor Q_1.

In Phase-splitter we have transistor Q_2 which can be used to split the phase in HIGH & LOW [According to ON state or OFF state of Q_2 it will split the phase in 1 or 0]

In output stage, we have 2 transistors Q_1 & Q_4. Both Q_1 & Q_4 will never remain ON at the same time. Depending on which transistor will remain ON or OFF, the diode D_1 will be either forward or reversed biased.

This type of configuration is also called as TOTEM-POLE CONFIGURATION.

This particular configuration can be utilised as a NAND gate.

Advantage of Totem Pole

→ Less power dissipation

→ In high o/p, it act as emitter follower circuit i.e it will follow emitter-voltage as the o/p voltage.

Disadvantage

→ Fan-out can-not be achieved.

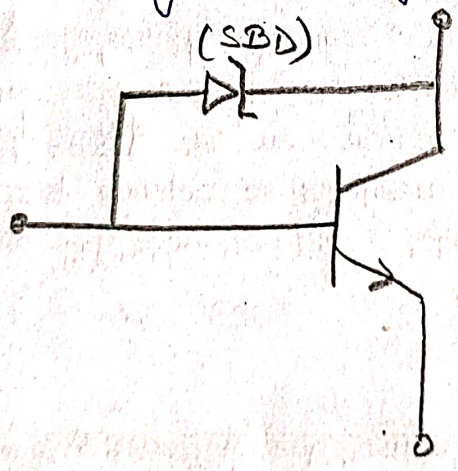
Schottky TTL

→ When a transistor is in saturation, a large number of charge carriers are present in collector

→ To switch this transistor into cut-off, all the charge carriers are needed to be removed from the collector, which takes a lot of time and thus decreases switching speed of the gate.

→ The delay is known as Saturation delay time and this delay can be reduced by using Schottky TTL.

→ A schottky diode is fabricated between base and collector of each circuit transistors of TTL which prevents the circuit transistor from saturating, thereby reducing switching time.



SBD – Schottky barrier diode

→ In Schottky TTL, a SBD is used which prohibit the transistor to enter into deep saturation.

→ The forward voltage of SBD is 0.25V only, so when transistor tries to go into saturation before that SBD becomes forward bias.

→ The current gets divided into transistor and diode and because of less base current the transistor cannot go into deep saturation.

→ As transistor can does not enter into deep saturation so the time required to remove charge carriers becomes less and switching speed get increased.

Complementary MOS Logic

→ Complementary Metal Oxide Semiconductor belongs to the Unipolar Logic families.

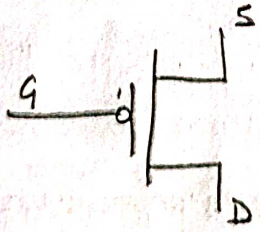
→ CMOS have very low power consumption, considerable resistance to noise and high packing density i.e large no. of circuits can be placed on the same chip.

→ CMOS behaves as an inverter.

→ In CMOS logic, both P-type and N-type MOS transistors are used on the same chip.

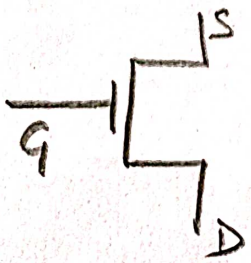
⇒ CMOS = PMOS and NMOS

PMOS



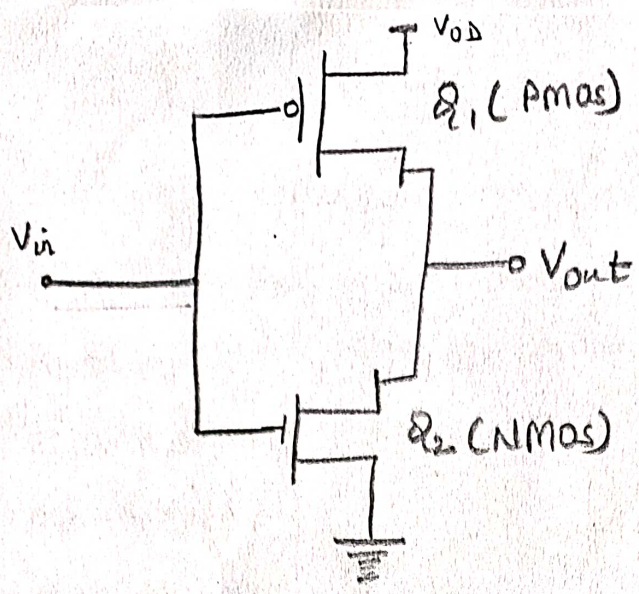
G = 0 → ON → SC
G = 1 → OFF → OC
} invert

NMOS



G = 0 → OFF - OC

G = 1 → ON - SC



CMOS = PMOS + NMOS

CMOS Inverter

V_{in}	Q_1	Q_2	V_{out}
0	ON	OFF	1
1	OFF	ON	0

Advantages

- Circuit is simple
- Fabricated in small area
- Power usage less
- Work on 5V-20V
- Power dissipation is low.

Disadvantage

- Propagation time is more (70ns)
- Cost is more than TTL.

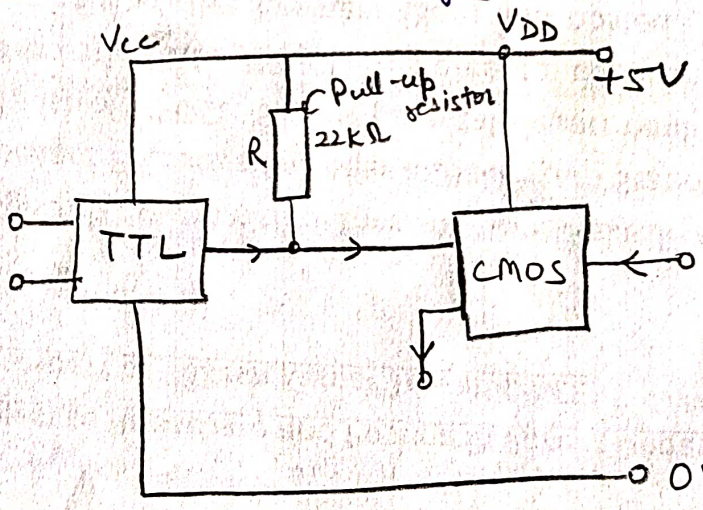
Interfacing CMOS and TTL

To achieve optimum performance in a digital system, devices from more than one logic family can be used, taking advantages of the superior characteristics of each family for different parts of the system.

Ex- CMOS logic ICs can be used in the system where low power dissipation is required whereas TTL can be used for those where high speed of operation is required.

Therefore interfacing between CMOS and TTL devices is needed.

TTL to CMOS interfacing



Pull-up resistor raises the output level of TTL to above +5V in the HIGH state.

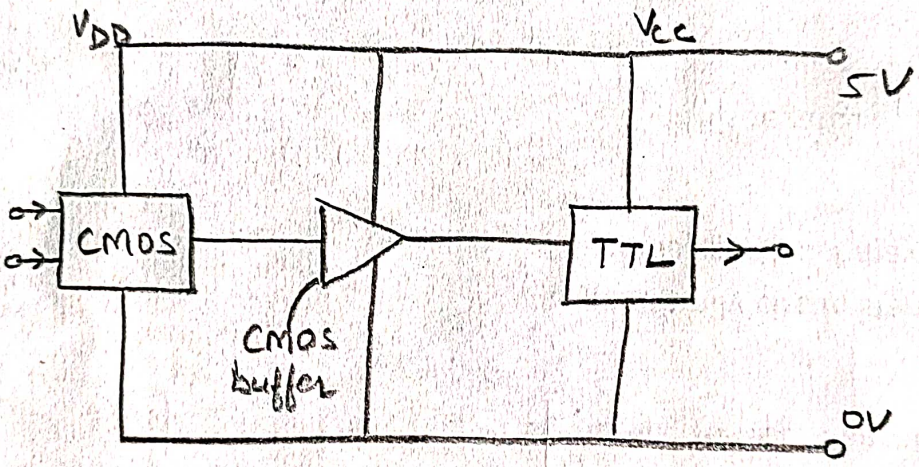
→ When we interface different types of ICs, it is necessary to check whether the driving IC is capable of meeting the current and voltage requirements of the load IC or not.

→ When 5V supply is given to TTL and CMOS ICs, logic levels of TTL and CMOS are different.

→ One TTL IC can drive any number of CMOS ICs. However, TTL output in 'high state' yields 2.4 Volts which is lower than the minimum voltage required by CMOS IC.

→ For TTL to CMOS interfacing standard pull-up resistor is connected which solves the interfacing problem.

CMOS to TTL interfacing



→ A CMOS IC can easily drive any low power Schottky TTL IC directly.

→ In CMOS to TTL interfacing, current level compatibility needs attention.

→ In the LOW state, the output current-sinking capability of CMOS IC must be atleast equal the input current-sinking requirement of the TTL IC.

→ Similarly, in the HIGH state, the HIGH output current drive capability of CMOS IC must equal or exceed the HIGH level input current requirement of TTL IC.